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| 10/646,076 | 08/22/2003 | John S. Montrym | NVID-P000705 | 9603 |

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| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/646,076 | MONTRYM ET AL. |
| | Examiner | Art Unit | |
| | Joni Hsu | 2628 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>22 January 2007</u>.

2a)☐ This action is **FINAL**.     2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-25 and 27-44</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-23,25,27-35 and 38-42</u> is/are rejected.

7)☒ Claim(s) <u>24,36,37,43 and 44</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1.  A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on January 22, 2007 has been entered.

### *Response to Arguments*

2.  Applicant's arguments with respect to claims 1-23, 25, 27-35, and 38-42 have been

considered but are moot in view of the new ground(s) of rejection.

3.  Applicant's arguments, see pages 14-21, filed January 22, 2007, with respect to the

rejection(s) of claim(s) 28-31 under 35 U.S.C. 102(b) and claims 1-23, 25, 26, 27, 32-35, and 38-

42 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of

rejection is made in view of Fuchs and Johns (US006366289B1).

4.  With regard to Morein (US006188394B1), Applicant argues that Morein teaches that a

single address is identified by a pointer stored at a location corresponding to a pixel, and as such,

Morein teaches away by from the claimed embodiments by teaching that a single address is

identified instead of transforming the received address into multiple subpixel addresses (page 14).

In reply, the Examiner agrees that Morein does not teach transforming the received address into multiple subpixel addresses. However, new grounds of rejection are made in view of Fuchs.

Applicant argues that Morein does not teach that at least two subpixels are read using such multiple subpixel addresses. Morein teaches that data can be retrieved based upon a determination of whether a compressed sample set or a pointer is stored in a memory, but fails to teach that the data is read (page 15).

In reply, the Examiner points out that since Morein teaches that the data can be retrieved, this means that the data is read. However, the Examiner agrees that Morein does not teach that multiple subpixel addresses are used to read at least two subpixels. However, new grounds of rejection are made in view of Fuchs.

5.     With regard to Sturges (US005854637A), Applicant argues that Sturges teaches a virtual frame buffer device, which is a device running on a CPU instead of a virtual frame buffer comprising memory addresses as claimed. Sturges teaches a shared memory comprising a predefined memory range which forms a frame buffer. As such, Sturges teaches away from the claimed embodiments by teaching a memory range forming a frame buffer instead of a virtual frame buffer (page 17). Additionally, Sturges further teaches away from the claimed embodiments by teaching that the memory range is that of a shared memory instead of a graphics memory (page 18).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of

Johns.

6.      Applicant's arguments, see page 21, filed January 22, 2007, with respect to Claims 24

and 36 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims

24 and 36 has been withdrawn.

### *Claim Objections*

7.      Claim 2 is objected to because of the following informalities: Claim 2 ends with a colon.

According to MPEP 608.01(m), each claim must end with a period. Appropriate correction is

required.

8.      Claim 44 is objected to because of the following informalities: Claim 44 recites "..being

equal to a *the* pitch of the frame buffer..." where it should recite "being equal to a pitch of the

frame buffer..." Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

9.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the subject
> matter sought to be patented and the prior art are such that the subject matter as a whole
> would have been obvious at the time the invention was made to a person having ordinary
> skill in the art to which said subject matter pertains. Patentability shall not be negatived
> by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-4, 9, 10, 13, 15-17, 19, 21-23, and 32-35 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Morein (US006188394B1) in view of Johns (US006366289B1).

12. With regard to Claim 1, Morein describes a method for providing antialiased memory

access (*storing antialiasing pixel data*, Col. 2, lines 46-47; *it is determined whether a*

*compressed sample set or a pointer is stored in the primary memory for a particular pixel, and*

*then the data can be retrieved based on that determination*, Col. 4, lines 9-13), comprising

receiving a request to access a memory address (Col. 4, lines 9-13); and transforming the

memory address into at least one physical address within a frame buffer utilized for antialiasing

(*a pointer is stored at the frame buffer location corresponding to the particular pixel, the pointer*

*points to a selected address in a sample memory at which the complete sample set for the pixel is*

*stored*, Col. 2, lines 19-23), wherein the frame buffer (sample memory 38) is a single memory

for containing data of a plurality of subpixels (samples) corresponding to a pixel of frame buffer

36 (*each pixel is described by a number of samples*, Col. 2, lines 19-23, 25-31); and accessing

data of a subpixel at the at least one physical address within the frame buffer (*data is retrieved by the pointer stored in the frame buffer*, Col. 4, lines 9-13).

However, Morein does not teach that frame buffer 36 is a virtual frame buffer and determining if the memory address is within a virtual frame buffer and, if so, performing the transforming and accessing. However, Johns discloses determining if the memory address is within a virtual frame buffer and, if so, performing the transforming and accessing (*VFB controller emulates a frame buffer residing in the address space of the host computer's system bus, referred to as the virtual frame buffer, this virtual address space, display controller emulates a virtual frame buffer by re-directing read and write requests to the linear address space of the virtual frame buffer to a physical address*, Col. 16, lines 15-23, 55-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Morein to include a virtual frame buffer device as suggested by Johns because Johns suggests that the display image being managed as the virtual frame buffer appears as if it resides in the frame buffer address space, but in actuality, the display image is sub-divided into chunks distributed randomly in memory (Col. 6, lines 58-61), which requires less memory than a conventional frame buffer (Col. 2, lines 11-14, 53-66).

13.    With regard to Claim 2, Morein does not teach accessing data at the memory address provided the memory address is not within the virtual frame buffer. However, Johns describes that if the memory address is within a virtual frame buffer, the memory address is transformed into a physical address within a frame buffer, and the driver manages the memory to access data at the physical address within a frame buffer (*VFB controller emulates a frame buffer residing in*

*the address space of the host computer's system bus, referred to as the virtual frame buffer, this*

*virtual address space, display controller emulates a virtual frame buffer by re-directing read and*

*write requests to the linear address space of the virtual frame buffer to a physical address,* Col.

16, lines 15-23, 55-67). If the memory address is not within the virtual frame buffer, then the

driver manages the memory to access data at the memory address (*driver can implement function*

*calls to perform operations on images managed in the frame buffer address space (or outside*

*this address space),* Col. 15, lines 56-62).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Morein to include accessing data at the memory address

provided the memory address is not within the virtual frame buffer as suggested by Johns

because Johns suggests the advantage of using the video memory for the frame buffer as well as

for other clients such as a compositor (Col. 7, lines 36-51; Col. 9, lines 31-33). If the video

memory is being accessed for the frame buffer, then it is advantageous to use a virtual frame

buffer, as discussed in the rejection for Claim 1. If the video memory is being accessed for other

clients such as a compositor, then the video memory can be directly accessed by the compositor

(Col. 8, lines 30-33).


14.     With regard to Claim 3, Morein does not teach that the virtual frame buffer comprises a

predefined memory range of a graphics memory. However, Johns discloses that the virtual

frame buffer comprises a predefined memory range of a graphics memory (310, Figure 3)

(*referred to as the virtual frame buffer, this virtual address space is depicted as the frame buffer*

*address space,* Col. 16, lines 15-23, 55-67; *driver can implement function calls to perform*

*operations on images managed in the frame buffer address space (or outside this address space)*,

Col. 15, lines 56-62; *VFB controller can manage requests to the local video memory device 310*,

Col. 7, lines 48-51). This would be obvious for the same reasons given in the rejection for Claim

2.

15.     With regard to Claim 4, Morein describes that the memory address is received from a

central processing unit (CPU) (82, Figure 4; Col. 8, lines 43-45).

16.     With regard to Claim 9, Claim 9 is similar to Claim 1, except that Claim 9 is for

accessing data in order to read data. Morein describes accessing data in order to read data (Col.

4, lines 9-13). Therefore, Claim 9 is rejected under the same rationale as Claim 1.

17.     With regard to Claim 10, Morein describes providing the subpixel value to a central

processing unit (CPU) (82, Figure 4; Col. 8, lines 43-52).

18.     With regard to Claim 13, Claim 13 is similar in scope to Claim 3, and therefore is

rejected under the same rationale.

19.     With regard to Claim 15, Claim 15 is similar in scope to Claim 9, except Claim 15 is for

reading the plurality of subpixel values and combining the subpixel values. Morein describes

reading the plurality of subpixel (sample) values at the plurality of physical addresses within the

frame buffer (38, Figure 2; Col. 4, lines 9-13; Col. 2, lines 19-23) and combining the subpixel

values to generate a pixel value for the specific pixel (Col. 2, lines 25-31). Therefore, Claim 15
is rejected under the same rationale as Claim 9.

20.    With regard to Claim 16, Morein describes providing the pixel value to a central

processing unit (CPU) (82, Figure 4; Col. 8, lines 21-25).

21.    With regard to Claim 17, Morein describes that the combining comprises blending the

subpixel values into a single color value (Col. 2, lines 25-31).

22.    With regard to Claim 19, Claim 19 is similar in scope to Claim 3, and therefore is

rejected under the same rationale.

23.    With regard to Claim 21, Claim 21 is similar to Claim 1, except that Claim 21 is for

accessing data in order to write data. Morein describes accessing data in order to write data (Col.

2, lines 15-19). Therefore, Claim 21 is rejected under the same rationale as Claim 1.

24.    With regard to Claims 22 and 23, these claims are similar in scope to Claims 2 and 3

respectively, and therefore are rejected under the same rationale.

25.    With regard to Claim 32, Morein describes receiving an address in frame buffer 36 from

the computer program (Col. 5, lines 39-48; Col. 9, line 64-Col. 10, line 20); transforming the

received address into at least one subpixel (sample) address (Col. 5, lines 39-48; Col. 5, line 59-

Col. 6, line 2), the subpixel address being an address into a frame buffer (sample memory 38)

which is a single memory storing data of a plurality of subpixels corresponding to each pixel of

frame buffer 36 (Col. 2, lines 19-23, 25-31); reading at least two subpixels from the frame buffer

(sample memory 38) using the subpixel address (Col. 4, lines 9-14); blending the at least two

subpixels to create a pixel value (Col. 2, lines 25-31); supplying the created pixel value to the

computer program as if it were a pixel value located at the received address in frame buffer 36;

and wherein the computer program does not directly access the frame buffer (sample memory

38) (Col. 4, lines 9-14).

However, Morein does not teach that frame buffer 36 is a virtual frame buffer, and

supplying a base address and buffer size information corresponding to a virtual frame buffer.

However, Johns discloses a method for supplying a virtual frame buffer to a computer program,

comprising supplying a base address and buffer size information to the computer program, the

base address and the buffer size information corresponding to a virtual frame buffer (*VFB*

*controller reads the base address*, Col. 10, lines 27-30; *upper left corner of the virtual frame*

*buffer (address 0) always starts at the lowest address of the frame buffer, offset may be equal to*

*(width\*BPP)(width of the frame buffer in bytes times the number of bytes per pixel)*, Col. 16,

lines 34-44); receiving an address in the virtual frame buffer from the computer program (*VFB*

*logic extracts the address of a pixel in the virtual buffer*, Col. 16, lines 59-64); transforming the

received address (*VFB logic converts the linear address of a location in the virtual frame buffer*

*to an address of a pixel in a decompressed chunk stored in physical memory*, Col. 17, lines 1-3);

reading data using the transformed address; supplying the data to the computer program as if it

were a pixel value located at the received address in the virtual frame buffer; and wherein the

computer program does not directly access the frame buffer (*view that the virtual frame buffer provides to application and system software running on the host CPU, to the host, the display image appears to reside in a linear address space, in actuality the display image is sub-divided into chunks distributed randomly in memory*, Col. 6, lines 52-61).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein to include supplying a base address and buffer size information corresponding to a virtual frame buffer as suggested by Johns. Johns suggests that the base address is needed in order to know where the frame buffer starts, and all the addresses can be calculated by adding a certain offset to the base address, which simplifying the calculation of which chunk contains a requested pixel address. The buffer size is needed in order to calculate the correct address (Col. 16, lines 34-44). The advantages of using a virtual frame buffer were discussed in the rejection for Claim 1.

26.     With regard to Claim 33, Morein does not teach that the computer program is an operating system. However, Johns describes that the computer program is an operating system (35, Figure 1) (*program modules including an operating system 35*, Col. 4, lines 64-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein so that the computer program is an operating system as suggested by Johns because Johns suggests that it is well-known in the art to use operating system software to perform operations on memory (Col. 1, lines 42-51).

27.    With regard to Claim 34, Morein does not teach that the computer program is a software

driver.  However, Johns describes that the computer program is a software driver (*driver is*

*responsible for memory management functions*, Col. 13, lines 8-20).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Morein so that the computer program is a software driver as

suggested by Johns because Johns suggests that using a software driver allows the host to choose

the memory management scheme (Col. 13, lines 8-20), making the memory manage scheme

more flexible.


28.    With regard to Claim 35, Morein describes that the computer program (84, Figure 4) is an

application program (Col. 8, lines 16-21).


29.    Claims 5, 6, 11, 12, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Morein (US006188394B1) and Johns (US006366289B1) in view of Dye (US005664162A).


30.    With regard to Claim 5, Morein and Johns are relied upon for the teachings as discussed

above relative to Claim 4.

However, Morein and Johns do not teach providing the CPU with a pitch value of the

frame buffer.  However, Dye describes providing the CPU (128, Figure 1) with a pitch value of

the frame buffer (110) (*CPU 128 controls the system bus 102 for providing data and*

*instructions, host CPU 128 asserts address signals*, Col. 7, lines 59-66; *host data bus transfers*

*data and instructions to and from the host computer system, which includes the host CPU 128,*

Col. 9, lines 59-64; *pitch of the frame buffer 110,* Col. 12, lines 10-17).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Morein and Johns to include providing the CPU with a pitch value of the frame buffer as suggested by Dye because Dye suggests that the CPU needs to know the pitch value of the frame buffer in order to read data from the correct location corresponding with the virtual frame buffer (116) (Col. 3, lines 49-51; Col. 12, lines 1-24).

31.     With regard to Claim 6, Morein does not teach the CPU calculating a physical address within the frame buffer using the pitch value of the frame buffer as the pitch of the virtual frame buffer. However, Dye describes the CPU (128, Figure 1) calculating a physical address within the frame buffer (110) using the pitch value of the frame buffer as the pitch of the virtual frame buffer (116) (*private memory is virtual frame buffer,* Col. 3, lines 49-51; Col. 12, lines 1-24). This would be obvious for the same reasons given in the rejection for Claim 5.

32.     With regard to Claim 11, Claim 11 is similar in scope to Claim 5, and therefore is rejected under the same rationale. With regard to Claims 12, 18, and 25, these claims are all similar in scope to Claim 6, and therefore are rejected under the same rationale.

33.     Claims 7, 8, 14, 20, 27, and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Johns (US006366289B1) in view of Baldwin (US005594854A).

34.    With regard to Claim 7, Morein and Johns are relied upon for the teachings as discussed

above relative to Claim 1.

However, Morein and Johns do not teach that the plurality of subpixels corresponding to

the pixel of the virtual frame buffer have physical addresses that are nearby each other.

However, Baldwin describes that the buffer must reside at contiguous physical addresses, and if

the virtual memory buffer maps to non-contiguous physical memory, then the buffer must be

divided into sets of contiguous physical memory pages (Col. 18, lines 45-52). Therefore, the

plurality of subpixels (Col. 34, lines 61-67) corresponding to the pixel of the virtual frame buffer

have physical addresses are nearby each other (Col. 18, lines 35-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by

applicant to modify the devices of Morein and Johns so that the plurality of subpixels

corresponding to the pixel of the virtual frame buffer have physical addresses that are nearby

each other as suggested by Baldwin because Baldwin suggests that this is needed because the

data in the physical memory needs to be transferred together (Col. 18, lines 35-52).


35.    With regard to Claim 8, Morein does not teach that the physical addresses are also based

on a base physical address which corresponds to the memory address. However, Johns describes

that the physical addresses are also based on a base physical address which corresponds to the

memory address (*VFB controller reads the base address of the chunk from the pointer list and*

*calculates the pixel offset in the chunk based on the incoming linear address, after computing the*

*address of the pixel within an uncompressed chunk, the VFB performs the requested read or*

*write operation on the pixel's address in physical memory,* Col. 10, lines 26-35).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Morein so that the physical addresses are also based on a base

physical address which corresponds to the memory address as suggested by Johns because Johns

suggests that a base physical address is needed as the reference starting point, and all the

addresses can be determined by their offsets from the base physical address (Col. 10, lines 26-

35).

36.   With regard to Claims 14, 20, 27, and 38, these claims are similar in scope to Claims 8,

14, 20, and 7 respectively, and therefore are rejected under the same rationale.

37.   With regard to Claim 39, Claim 39 is similar in scope to Claim 32 except that Claim 39 is

for writing the pixel value and the plurality of subpixels comprise nearby physical addresses.

Morein describes writing the pixel value (Col. 2, lines 15-19).

However, Morein does not teach that the plurality of subpixels comprise nearby physical

addresses. However, Baldwin describes that the buffer must reside at contiguous physical

addresses, and if the virtual memory buffer maps to non-contiguous physical memory, then the

buffer must be divided into sets of contiguous physical memory pages (Col. 18, lines 45-52).

Therefore, the plurality of subpixels (Col. 34, lines 61-67) corresponding to the pixel of the

virtual frame buffer have physical addresses are nearby each other (Col. 18, lines 35-52), as

discussed in the rejection for Claim 7.

38.    With regard to Claims 40-42, these claims are similar in scope to Claims 33-35

respectively, and therefore are rejected under the same rationale.

39.    Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein

(US006188394B1) in view of Fuchs.

40.    With regard to Claim 28, Morein describes a method for reading a frame buffer (sample

memory 38, Figure 2; *a pointer is stored at the frame buffer location corresponding to the*

*particular pixel, the pointer points to a selected address in a sample memory at which the*

*complete sample set for the pixel is stored*, Col. 2, lines 19-23; *it is determined whether a*

*compressed sample set or a pointer is stored in the primary memory for a particular pixel, and*

*then the data can be retrieved based on that determination*, Col. 4, lines 9-13), the method

comprising receiving an address corresponding to a pixel (*pointer is stored at the frame buffer*

*location corresponding to the particular pixel*, Col. 2, lines 18-20); transforming the received

address into at least one subpixel (sample) address (*pointer points to a selected address in a*

*sample memory at which the complete sample set for the pixel is stored*, Col. 2, lines 20-23; *each*

*pixel is described by a number of samples*, Col. 2, lines 25-31); reading at least two subpixels

from the frame buffer using at least one subpixel address (*sample set is retrieved by the pointer*

*stored in the frame buffer*, Col. 4, lines 9-13), wherein the frame buffer is a single memory

comprising a plurality of pixels, wherein each pixel comprises a plurality of subpixels (*sample*

*memory 38 stores a plurality of pixel entries, and each of the pixel entries stores the plurality of*

*pixel samples*, Col. 5, lines 44-47; Col. 2, lines 25-31); and blending the at least two subpixels to create a pixel value for the pixel (*samples are combined to produce a resultant color value for the particular pixel*, Col. 2, lines 25-31). Morein discloses that the frame buffer stores an uncompressed set of subpixels (Col. 5, lines 57-63).

However, Morein does not teach transforming the received address into multiple subpixel addresses; using at least two of the multiple subpixel addresses to read at least two subpixels. However, Fuchs discloses transforming the received address (x, y) into multiple subpixel addresses (x+xoffset, y+yoffset); using at least two of the multiple subpixel addresses to read at least two subpixels (*each pixel (x,y), is subdivided into a grid of subpixels so that each subpixel has an address of the form (x+xoffset, y+yoffset), sample points within a pixel's area*, page 119, second column, fourth paragraph).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Morein to include transforming the received address into multiple subpixel addresses; using at least two of the multiple subpixel addresses to read at least two subpixels as suggested by Fuchs because Fuchs suggests the advantage of knowing the location of the sample points within the pixel at which to sample in order to perform anti-aliasing (page 119, second column, third and fourth paragraphs).

41.     With regard to Claim 29, Morein describes supplying the pixel value as if it were a pixel value at the received address (Col. 4, lines 6-14).

42.    With regard to Claim 30, Morein describes a method for writing a frame buffer (38,

Figure 2) comprising receiving an address and a pixel value from a computer program (84,

Figure 4; Col. 2, lines 19-21; *instructions 84 which cause the controller 82 to perform a*

*predetermined function, the instructions 84 may be a software algorithm, receiving a pixel*

*fragment,* Col. 8, lines 15-27), the computer program supplying the address and pixel value as if

accessing a frame buffer that does not comprise subpixels (samples); transforming the received

address into at least one subpixel address; writing the pixel value to a frame buffer as multiple

subpixel values using the at least one subpixel address (Col. 2, lines 19-23, 25-31) wherein the

frame buffer is a single memory comprising a plurality of pixels (Col. 5, lines 44-47) wherein

each pixel comprises a plurality of subpixels (Col. 5, lines 39-44).

However, Morein does not teach transforming the received address into multiple subpixel

addresses; and writing the pixel value as multiple subpixel values using the multiple subpixel

addresses. However, Fuchs discloses transforming the received address into multiple subpixel

addresses; and writing the pixel value as multiple subpixel values using the multiple subpixel

addresses (page 119, second column, fourth paragraph). This would be obvious for the same

reasons given in the rejection for Claim 28.

43.    Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein

(US006188394B1) and Fuchs in view of Toji (US007158148B2).

Morein and Fuchs are relied upon for the teachings as discussed above relative to Claim

30.

However, Morein and Fuchs do not teach modifying at least one of the multiple subpixel

values in the frame buffer based upon a pixel value of a surrounding pixel. However, Toji

discloses modifying at least one of the multiple subpixel values in the frame buffer based upon a

pixel value of a surrounding pixel (*when a mismatch in the data of the sub-pixels constituting the*

*target pixel and the data of the sub-pixels constituting the pixels adjacent to the target pixel*

*occurs, then said control unit performs correction in order to eliminate the mismatch*, Col. 40,

lines 40-47).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the devices of Morein and Fuchs to include modifying at least one of the

multiple subpixel values in the frame buffer based upon a pixel value of a surrounding pixel as

suggested by Toji because Toji suggests the advantage of allowing a smoother image to be

displayed (Col. 2, lines 58-65).

## *Allowable Subject Matter*

44.     Claims 24, 36, 37, 43, and 44 objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

45.     The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a method comprising

transforming a received address into at least one subpixel address, the subpixel address being an

address into a frame buffer which is a single memory storing data of a plurality of subpixels

corresponding to each pixel of a virtual frame buffer; wherein the base address of the virtual

frame buffer is the same as a base address of the frame buffer, as recited in Claims 24 and 36.

Claim 37 depends from Claim 36, and therefore also contains allowable subject matter.

The prior art also does not teach a method comprising transforming a received address

into at least one subpixel address, the subpixel address being an address into a frame buffer

which is a single memory storing data of a plurality of subpixels corresponding to each pixel of a

virtual frame buffer and wherein the plurality of subpixels comprise nearby physical addresses;

wherein the base address of the virtual frame buffer is the same as a base address of the frame

buffer, as recited in Claims 43 and 44.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The

examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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applications is available through Private PAIR only. For more information about the PAIR

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like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


JH


Ulka Chauhan

Supervisory Patent Examiner